Available online at www.sciencedirect.com
SCIENCE DIRECT®

Journal of the European Ceramic Society 24 (2004) 1459–1462

www.elsevier.com/locate/jeurceramsoc

High carrier density CeO_2 dielectrics—implications for MOS devices

Jyrki Lappalainen[a,b,*], Darja Kek[b,c], Harry L. Tuller[b]

[a]*Microelectronics and Materials Physics Laboratory, PO Box 4500, FIN-90014 University of Oulu, Finland*
[b]*Crystal Physics and Electroceramics Laboratory, Department of Material Science and Engineering, Massachusetts Institute of Technology, 77 Massachusetts Avenue, Cambridge, MA 02139, USA*
[c]*Jozef Stefan Institute, Jamova 39, SI-1000 Ljubljana, Slovenia*

Received 19 September 2002; received in revised form 8 November 2002

Abstract

Nanocrystalline CeO_2 films of 75 nm thickness were deposited on *n*-type (100) silicon substrates using pulsed laser deposition (PLD) technique to form a gate dielectric in the Pt/Si/CeO_2/Pt MOS capacitor. XRD and AFM were used for characterization of the film crystal structure and grain size. Electrical properties of the MOS structure were examined by capacitance–voltage (C–V) and impedance spectroscopy measurements. Based on the impedance measurements and reported electron mobilities, we derive a rather high carrier density of the order of 6×10^{17} cm^{-3}. Nevertheless, their overall high resistance enables the films to serve as dielectrics. In contrast to conventional MOS capacitors, we find an additional capacitive contribution under accumulation we attribute to the electron depletion in the CeO_2 film. We present a model consistent with these results.

Keywords: Capacitor; CeO_2; Electrical properties; Films; Microstructure

1. Introduction

The continued drive towards ever smaller submicron lateral dimensions in MOSFET technology has pushed the SiO_2 gate oxide thickness to the order of nanometers leading, in turn, to higher leakage currents and processing difficulties. Replacement of the SiO_2 films by thicker films with higher dielectric constants compared with SiO_2 ($\varepsilon_r\approx3.5$) promises equivalent capacitances with reduced leakage and threat of electrical breakdown.[1] Cerium dioxide (CeO_2) appears to be a particularly attractive candidate, given its high dielectric constant ($\varepsilon_r\approx25$) and its compatibility with Si. In the solid state ionics arena, there is much interest in reducing the operating temperatures of solid state oxide fuel cells (SOFC) by shifting from bulk to thin film electrolytes (stabilized ZrO_2 or acceptor doped CeO_2). The lattice constant mismatch between diamond-structured silicon and fluorite-structured CeO_2 is only about 0.35%, thus enabling the fabrication and deposition of stress free, highly oriented or epitaxial thin film structures. Furthermore, CeO_2 forms no undesirable reaction products, such as silicides, when in contact with silicon at elevated temperatures.[2–4] Lastly, CeO_2 thin films are effective as buffer layers and diffusion barriers between the Si substrate and many complex and chemically reactive compounds, such as Pb(Zr,Ti)O_3 and $PbTiO_3$.[5–7] In this paper we describe the fabrication and characterization of the Pt/Si/CeO_2/Pt MOS device structure. The electrical properties of the CeO_2 thin films are deconvoluted from the overall response of the MOS device with the assistance of impedance spectroscopy. The analysis reveals an interesting new property of the MOS device based on the features of high carrier density CeO_2 dielectrics.

2. Experimental

CeO_2 thin films were deposited onto *n*-type silicon wafers by a pulsed KrF excimer laser (Lambda Physik LPX-300) operating at a wavelength of 248 nm. The laser pulse energy was 400 mJ, with the beam fluence set to 3.65 J/cm^2 with aid of focusing optics. In situ deposition was carried out in a vacuum chamber 1.5×10^{-3} Torr at the temperature of 600 °C. *n*-Type silicon substrates with resistivity of 2–4 Ωcm and (100) surface orientation were placed parallel to the target at a distance of 65 mm from the target surface. Before deposition, the silicon substrates were etched with 5% HF in water and rinsed with deionized water. Both back

* Corresponding author. Tel.: +358-8-553-2720; fax: +358-8-553-2728.
E-mail address: jyla@ee.oulu.fi (J. Lappalainen).

0955-2219/$ - see front matter © 2003 Elsevier Ltd. All rights reserved.
doi:10.1016/S0955-2219(03)00578-8

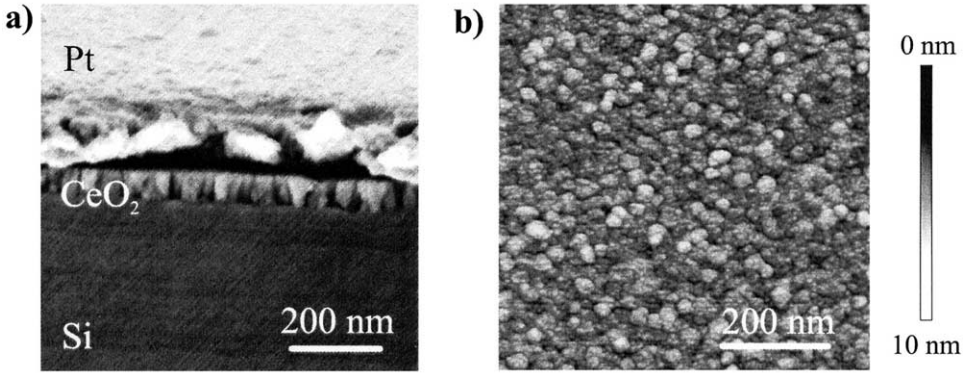

Fig. 1. (a) FESEM cross section micrograph of a Pt/Si(100)/CeO_2/Pt structure and (b) AFM micrograph of CeO_2 thin-film surface. Columnar structure of the CeO_2 film in (a) is clearly evident.

and top platinum electrodes with thickness of 150 nm, and area of 130×10^{-6} and 2.405×10^{-6} m^2, respectively, were deposited by room temperature DC sputtering. Back electrode entirely covered the backside of the sample.

The CeO_2 target preparation included cold pressing pure CeO_2 powder at a pressure of 20 MPa, vacuum sealing the resultant pellet, followed by isostatic pressing at 290 MPa. After sintering at 1425 °C for 10 h in air, the target had a density of 6.5×10^3 kg/m^3. X-ray diffraction θ–2θ measurements (Rigaku RU300) were performed on both CeO_2 films and target. A tapping mode AFM (Nanoscope IIIa) and SEM (Jeol JSM-6400) were used for the evaluation of thin film surface quality. In order to study the electrical properties of the MOS structure, an impedance analyzer with frequency sweep from 0.1 Hz to 1 MHz (Solartron 1260) was used for both the complex impedance spectroscopy and C–V measurements.

3. Results and discussion

SEM and AFM micrographs of the Si(100)/CeO_2/Pt multilayer cross section and the CeO_2 thin-film surface are shown in Fig. 1(a) and (b), respectively. Analysis of X-ray diffraction measurements show the films to be mainly (111) oriented. Some contributions from (311) planes and reduced peak intensities suggest a reduced level of order when compared to epitaxial (111) oriented films.[8] In Fig. 1(a), a columnar grain structure of the CeO_2 films is clearly revealed. AFM micrograph of the sample presented in Fig. 1(a) is shown in Fig. 1(b). Analysis of this micrograph revealed a rms roughness value of $R_q\approx0.63$ nm. Also, from larger scale AFM micrographs, it was possible to estimate the grain size to be ~40 to 50 nm and to conclude that no large particulates were present, pointing to the high quality target used in the deposition process.

In order to correctly interpret the electrical response of the multilayer MOS device, one has to carefully consider the responses arising from the different regions of the device. For example, the potentially blocking nature of the Pt/Si and CeO_2/Pt contacts (work function differences: $\Phi_{Pt/Si} = 1.05$ eV and $\Phi_{CeO_2/Pt} = 0.6$ eV),[9] must to be taken into consideration as extra voltage-dependent capacitors connected in series with the dielectric film capacitance C_{ox}. In similar manner, one has to consider the space charge barrier layer resistance and capacitance at the Si/CeO_2 interface when interpreting the impedance spectrum. In Fig. 2(a) and (b), a

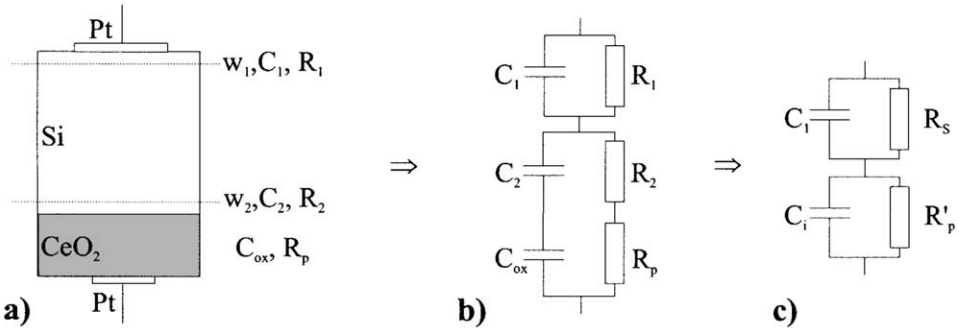

Fig. 2. Schematic drawing of the MOS device describing (a) the different space charge capacitances and resistances C_1, R_1 and C_2, R_2, and the oxide capacitance and resistance C_{ox}, R_p together with corresponding equivalent circuit in (b). In (c) the equivalent circuit is rearranged to accent the responses of the capacitances C_2 and C_{ox} typically studied in C–V measurements.

schematic structure of the MOS device and its equivalent circuit are sketched, respectively. In order to emphasize the important contributions for the C–V analyses, the equivalent circuit was rearranged according the Fig. 2(c) leading to the following equation for the impedance of the MOS structure:

$$Z = \left[\frac{R_s}{1+\omega^2 C_i^2 R_S^2} + \frac{R'_p}{1+\omega^2 C_i^2 R'^2_p}\right] - j\left[\frac{\omega C_1 R_S^2}{1+\omega^2 C_i^2 R_S^2} + \frac{\omega C_i R'^2_p}{1+\omega^2 C_i^2 R'^2_p}\right] = Z' + jZ''. \quad (1)$$

Since the dielectric constant of the silicon substrate is only 11.8 compared with that of the CeO_2 with $\varepsilon_r \sim 25$, and the thickness of the substrate is 500 μm compared with 75 nm of the film, respectively, the applied DC bias actually vanishes across the substrate space charge regions. Especially, in the state of accumulation, when the effect of C_2 in Fig. 2 disappears, C_1 can be estimated from the expression for the Schottky-junction capacitance.[10] An approximate value for the oxide resistance $R'_p = 12.6$ kΩ was derived from the impedance spectroscopy measurements. The resistance $R_s = 100$ MΩ was obtained as a function of the applied DC bias from impedance measurements carried out for the reference component without a CeO_2 thin film, i.e., Pt/Si/Pt. This resistance is not independent of DC bias, but represents typical values for back-to-back Schottky junction devices.

In Fig. 3, there are three C–V curves presented for a Pt/Si(100)/CeO_2/Pt MOS device measured at 100 Hz, 1 kHz, and 100 kHz, respectively. First of all, there are both depletion-inversion and accumulation plateaus shown in each C–V curve typical for MOS devices. At the frequencies of 100 Hz and 1 kHz, a value of 0.2 nF for the space charge capacitance C_2 in depletion was measured. This is very close to the calculated value of capacitance for an *n*-type silicon substrate with $N_d = 1.5\times10^{15}$ cm^{-3}. An oxide layer capacitance $C_{ox} = 6.5$ nF for CeO_2 in accumulation was also measured, giving a dielectric constant of $\varepsilon_r = 23$. There is also a clear shift of the flat band voltage V_{FB} to higher gate bias voltages with increasing frequency pointing to a contribution from interface traps. This shift of the flat band voltage might be pronounced due to the high concentration of defects in nonstoichiometric CeO_2 films with nanosized grains impairing the properties of the interface when compared, for example, with SiO_2/Si interface.[10] Furthermore, there is a slight increase in oxide capacitance C_{ox} with decreasing frequency. This, we believe, is a consequence of the heterogeneous Maxwell–Wagner effect typical for ceramics having grain boundaries with different conductivity than bulk grains. This effect is more prominent at frequencies below 100 Hz not shown here.[11] In addition to the conventional C–V measurement response, there were also some unusual features observed at low frequencies. Above a certain positive gate bias, there is a strong increase in the value of capacitance $C_i = (1/C_2 + 1/C_{ox})^{-1} \approx C_{ox}$ in accumulation shown in Fig. 3. This kind of behavior was found also by Sakai et al.[12] for a similar component structure with ohmic Al contacts, and they suggested that this increase was caused by leakage in CeO_2. However, we found this phenomenon to be strongly frequency

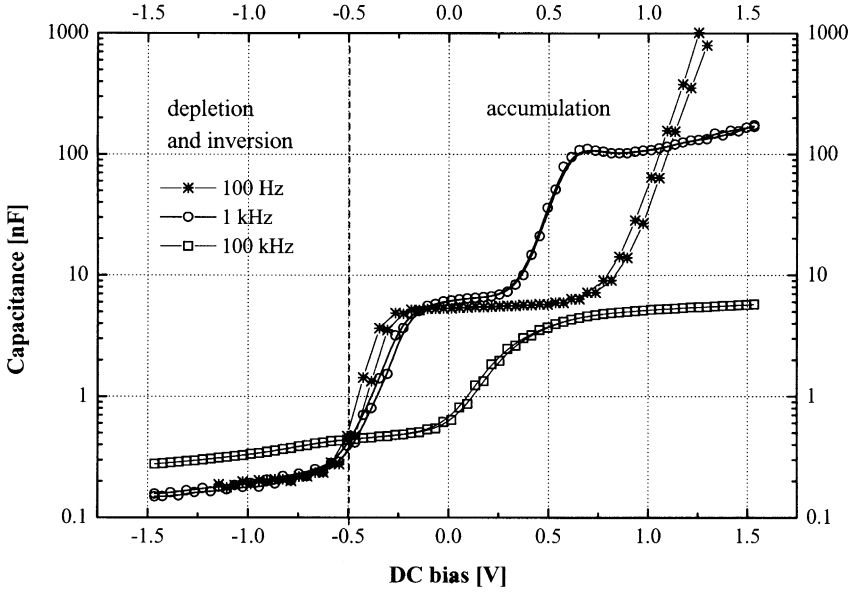

Fig. 3. Three C–V curves of a Pt/Si(100)/CeO_2/Pt device calculated from impedance spectroscopy data measured at 100 Hz, 1 kHz, and 100 kHz. Notice the second accumulation capacitance plateau in the curve measured at 1 kHz generated due to the depletion of the space charge in CeO_2.

dependent and thus probably related to space charge developed in the CeO_2 thin film, which might also cause leakage current under DC biasing conditions. At the frequency of 1 kHz, another plateau with capacitance of 100 nF was obtained. If one considers a biasing condition where the back-electrode Schottky barrier is totally reverse biased, the voltage drop across the depletion layer and the corresponding width of the depletion layer w_1 eventually saturates. When the gate potential is still increased, the back-electrode capacitance becomes meaningless in overall capacitance, and, thus, the second plateau of capacitance 100 nF in Fig. 3 must be located inside the CeO_2 film. The room temperature resistance of the CeO_2 film was $R'_p = 12.6\ k\Omega$ leading to a conductivity of $\sigma = 2.467\times10^{-8}$ S/cm. The electron density in the oxide can be estimated from knowledge of the published electron mobility. Using the measured activation energy $E_a = 0.45$ eV, a room temperature extrapolated electron mobility of $\mu = 2.8\times10^{-7}$ cm^2/Vs was calculated,[13] leading to an electron concentration of $n = 5.5\times10^{17}$ cm^{-3}. A low electron mobility, resulting form small polaron formation,[13] accompanied by the high charge carrier concentration in the CeO_2 thin film should certainly effect its film properties as a gate dielectric, due especially to the ease with which space charges may be activated inside the oxide. Since this space charge has a specific relaxation mechanism, its polarization response should be strongly frequency dependent, as is the case with these Pt/Si(100)/CeO_2/Pt structures. Indeed, there was a clear local maximum in loss angle $\tan\delta = 3.8$ at the frequency of 1 kHz and gate bias of around 0.6 V, whereas at 100 Hz, the loss angle was already indefinite, and at 100 kHz, the loss angle increased gently around a value of 0.6 without any resonance maximum with increasing gate bias. It is suggested here, that in the vicinity of this kind of resonance frequency, there is a voltage dependent depletion layer formed in the CeO_2 film near the silicon substrate interface leading to the unusual form of the C–V curves presented in Fig. 3. This capacitance increases strongly with decreasing DC bias under 0.6 V, which becomes evident also in C–V curves measured at 1 kHz in Fig. 3, behavior similar to that of the space-charge capacitance in back-electrode Schottky contact.

4. Conclusions

The fabrication and characterization of the Pt/Si/CeO_2/Pt MOS capacitor structure were described. The electrical properties of the CeO_2 thin films were characterized by examining and modeling the C–V response of the MOS structure utilizing conventional impedance spectroscopy. The CeO_2 layer was found to have a dielectric constant of $\varepsilon_r = 23$. A clear shift of the flat band voltage V_{FB} to the higher gate bias voltages with increasing frequency reflected a clear indication of the contribution of interface charge traps. In addition to the conventional C–V measurement response, there were also some unusual features observed at low frequencies. Above a certain positive gate bias, there is a strong increase in the value of capacitance C_{ox} in accumulation, which is most likely due to the space charge generation and depletion at higher DC bias voltages in the CeO_2 thin film. This is consistent with our findings of high electron densities in the CeO_2 films.

Acknowledgements

The authors acknowledge support from the NSF under grant DMR-9710699 and ARO-MURI under grant DAAD-0101-0566. D.K. thanks the support of the United States Government under Fulbright grant 25196. J.L. acknowledges the financial support by the Academy of Finland.

References

1. Li, M.-A., Wang, Z.-L., Fan, S.-S., Zhao, Q.-T. and Xiong, G.-C., Structural characteristics and the control of orientation of CeO_2 thin films prepared by laser ablation. *Nucl. Instrum. Meth.*, 1998, **B135**, 535–539.
2. Tsai, W.-C. and Tseng, T.-Y., Structural and electrical properties of cerium dioxide films grown by RF magnetron sputtering. *J. Mater. Sci. Mater. El.*, 1997, **8**, 313–320.
3. Jones, J. T., Croke, E. T., Garland, C. M., Marsh, O. J. and McGill, T. C., Epitaxial silicon grown on CeO_2/Si(111) structure by molecular beam epitaxy. *J. Vac. Sci. Technol.*, 1998, **B16**, 2686–2689.
4. Tye, L., El-Masry, N. A., Chikyow, T., McLarty, P. and Bedair, S. M., Electrical characteristics of epitaxial CeO_2 on Si(111). *Appl. Phys. Lett.*, 1994, **65**, 3081–3083.
5. Park, B.-E., Sakai, I., Tokumitsu, E. and Ishiwara, H., Hysteresis characteristics of vacuum-evaporated ferroelectric $PbZr_{0.4}Ti_{0.6}O_3$ films on Si(111) substrates using CeO_2 buffer layers. *Appl. Surf. Sci.*, 1997, **117–118**, 423–428.
6. Hirai, T., Teramoto, K., Nagashima, K., Koike, H. and Tarui, Y., Characterization on metal/ferroelectric/insulator/semiconductor structure with CeO_2 buffer layer. *Jpn. J. Appl. Phys.*, 1995, **34**, 4163–4166.
7. Wu, Y.-M. and Lo, J.-T., Dielectric properties of $PbTiO_3$ thin films on CeO_2/Si(111) and Y_2O_3/Si(100). *Jpn. J. Appl. Phys.*, 1998, **37**, 5645–5650.
8. Lappalainen, J., Kek, D. and Tuller, H. L., Investigation of Pt/Si/CeO_2/Pt MOS device structure by impedance spectroscopy. *Mat. Res. Soc. Symp. Proc.*, 2002, **699**, R5.1.1–R5.1.11.
9. Pfau, A., Schierbaum, K. D. and Göpel, W., The electronic structure of CeO_2 thin films: the influence of Rh surface dopants. *Surface Science*, 1995, **331–333**, 1479–1485.
10. Pierret, R. F., *Field Effect Devices*. Addison-Wesley, Boston, 1983.
11. Scaife, B. K. P., *Principles of Dielectrics*. Oxford Science Publications, New York, 1989.
12. Sakai, I., Tokumitu, E. and Ishiwara, H., Preparation and characterization of PZT thin films on CeO_2(111)/Si(111) structures. *Jpn. J. Appl. Phys.*, 1996, **35**, 4987–4990.
13. Tuller, H. L. and Nowick, A. S., Small polaron electron transport in reduced CeO_2 single crystals. *J. Phys. Chem. Solids*, 1977, **38**, 859–867.